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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FINDLEY, CHRISTOPHER G	
ART UNIT	**PAPER NUMBER**
2621	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,032	HATTI ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER FINDLEY	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6 and 8-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 3/24/2009 have been fully considered but they are not persuasive.

2. Re claims 9 and 11, the Applicant contends that the prior art cited fails to teach or suggest that "a portion of a picture stored in a frame buffer, the portion of the picture being stored with a pixel order" and "storing the portion of the picture in another buffer with the predetermined pixel order". However, the Examiner respectfully disagrees.

As previously stated, Baden discloses that Fig. 6 corresponds to the bridge/graphics controller 311 of Fig. 3, wherein the bridge/graphics controller 311 is connected to main memory subsystem 309 via a data bus 305. Accordingly, data bus 305 functions as the input to the schematic illustrated in Fig. 6 of Baden, and, therefore, main memory subsystem 309 may be considered a frame buffer.

The Applicant further contends that there is absolutely no teaching in Baden that the memory subsystem 309 stores a picture. While Baden includes no such explicit statement, Baden does disclose that a system bus in conventional computer graphics systems in the same field of endeavor as the prior art conveys both address and pixel data information (Baden: column 1, lines 21-23). Memory subsystem 309 and processor 307 are the only components explicitly shown as being connected along system data bus 305 of Fig. 3 in Baden. Since the input to the bridge/graphics controller 311 is coupled to the system data bus 305, as noted by the Applicant, one of ordinary skill in the art at the time of the invention would have found it obvious that

picture data is stored in the memory subsystem 309 because a processor by itself is does not store data, and therefore, in view of the disclosed figures of Baden, the memory subsystem 309 must store the data by default.

As a result of the reliance upon the knowledge of one of ordinary skill in the art to come to such a conclusion, the rejection has been modified so that claims 9-11 now stand rejected under 35 U.S.C. 103(a).

Claim Objections

3. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The Applicant has amended claim 4 to eliminate its dependency upon claim 3, but has not indicated another claim from which to draw its dependency. For the purposes of prior art examination, it is assumed that claim 4 is now dependent upon independent claim 1.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Baden et al. (US 5640545 A).

Re **claim 1**, Baden discloses a method for displaying pictures, said method comprising: fetching a portion of a picture being stored in a frame buffer, the portion of the picture stored with a byte order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data); converting the byte order of the portion of the picture to a predetermined byte order, the byte order being different from the predetermined byte order (Baden: Fig. 6, multiplexer 649; column 15, lines 51-55, the processor determines the byte order of the system data bus; column 16, lines 35-43, multiplexer 649 performs end-to-end byte swapping according to the mode of the input byte order in relation to the processor byte order); and storing the portion of the picture in another buffer with the predetermined byte order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data); and providing an indicator indicating whether the byte order is different or opposite from the predetermined order that the portion of the picture is converted (Baden: column 16, lines 50-53, the controller generates a little-endian or big-endian control signal, acting as a state machine, wherein the control signal is generated based on information about the processor mode, thus indicating whether a conversion is necessary).

Re **claim 2**, Baden discloses that the predetermined order is selected from a group consisting of big endian byte order and little endian byte order (Baden: column 15, lines 51-55, the processor determines big-endian (BE) or little-endian (LE) mode).

Re **claim 4**, Baden discloses swapping a first pixel from the portion of the picture and a second pixel from the portion of the picture if the indicator indicates that the byte order is different or opposite from the predetermined order (Baden: Fig. 1, illustrates a byte swapping operation; Figs. 2A-2B, bytes correspond to color pixels); and swapping a third pixel from the portion of the picture and a fourth pixel from the portion of the picture if the indicator indicates that the byte order is different or opposite from the predetermined order (Baden: Fig. 1, illustrates a byte swapping operation; Figs. 2A-2B, bytes correspond to color pixels).

Claim 5 recites the corresponding system for implementing the method of claim 1, and, therefore, has been analyzed and rejected with respect to claim 1 above.

Claim 6 has been analyzed and rejected with respect to claim 2 above.

Claim 7 has been analyzed and rejected with respect to claim 3 above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Baden et al. (US 5640545 A).

Re **claim 9**, Baden discloses a method for displaying pictures, said method comprising: fetching a portion of a picture stored in a frame buffer, the portion of the

picture being stored with a pixel order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data; Figs. 2A-2B, bytes correspond to color pixels); converting the pixel order of the portion of the picture to a predetermined pixel order (Baden: Fig. 6, multiplexer 649; column 15, lines 51-55, the processor determines the byte order of the system data bus; column 16, lines 35-43, multiplexer 649 performs end-to-end byte swapping according to the mode of the input byte order in relation to the processor byte order); and storing the portion of the picture in another buffer with the predetermined pixel order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data; Figs. 2A-2B, bytes correspond to color pixels).

While Baden does not explicitly disclose that memory subsystem 309 stores a picture, Baden does disclose that a system bus in conventional computer graphics systems in the same field of endeavor as the prior art conveys both address and pixel data information (Baden: column 1, lines 21-23). Memory subsystem 309 and processor 307 are the only components explicitly shown as being connected along system data bus 305 of Fig. 3 in Baden. Since the input to the bridge/graphics controller 311 is coupled to the system data bus 305, as noted by the Applicant, one of ordinary skill in the art at the time of the invention would have found it obvious that picture data is stored in the memory subsystem 309 because a processor by itself is does not store data, and therefore, in view of the disclosed figures of Baden, the memory subsystem 309 must store the data by default.

Re **claim 10**, Baden discloses rearranging a plurality of pixels from the portion of the picture in a plurality of different pixel orders (Baden: Fig. 6; Fig. 7A, multiplexer 649 has two inputs corresponding to little-endian byte order (input 0) and big-endian byte-order (input 1)); receiving an indicator indicating the pixel order (Baden: Fig. 7A, mode selection line 655); and selecting the pixels rearranged in one of the plurality of different pixel orders based on the indicator indicating the pixel order (Baden: column 16, lines 35-39).

Claim 11 recites the corresponding system for implementing the method of claim 9, and, therefore, has been analyzed and rejected with respect to claim 9 above.

8. Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baden et al. (US 5640545 A) in view of Wyland (US 6836869 B1).

Re **claim 8**, Baden discloses a majority of the features of claim 8 as discussed above, including performing an end-to-end byte swapping operation, but Baden does not specifically disclose a first multiplexer for selecting one of a first pixel of the portion of the picture and a second pixel of the portion of the picture; a second multiplexer for selecting another of the first pixel of the portion of the picture and a second pixel of the portion of the picture, from the first multiplexer; a third multiplexer for selecting one of a third pixel of the portion of the picture and a fourth pixel of the portion of the picture; a fourth multiplexer for selecting another of the third pixel of the portion of the picture and the fourth pixel of the portion of the picture, from the third multiplexer; a fifth multiplexer for multiplexing outputs from the first multiplexer, the second multiplexer, the third

multiplexer, and fourth multiplexer; and the selections of the first multiplexer, the second multiplexer, the third multiplexer, and the fourth multiplexer being controlled by the indicator provided by the state machine. However, Wyland discloses a byte swapping unit, wherein a 32-bit input stream is demultiplexed into four 8-bit bytes, and the bytes are fed into four 2-input multiplexers, so that the bytes may be swapped in an end-to-end manner based on a byte_endian_type control signal, whereby the output of the multiplexers are then recombined into a 32-bit stream (Wyland: Fig. 5A). Since both Baden and Wyland relate to performing byte swapping, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the multiplexer configuration of Wyland with the bridge/graphics controller of Baden in order to provide a system which is capable of operating in both an encoding/decoding mode and error correction mode while utilizing a single circuit configuration (Wyland: column 2, lines 14-17). The combined system of Baden and Wyland has all of the features of claim 8.

Re **claim 12**, Baden discloses a majority of the features of claim 11 as discussed above, including performing an end-to-end byte swapping operation, but Baden does not specifically disclose a demultiplexer for separating a plurality of pixels from the portion of the picture; a plurality of multiplexers for combining the separated plurality of pixels in a corresponding plurality of pixel orders; and another multiplexer for selecting an output from one of the plurality of multiplexers, based on an indicator indicating the pixel order provided by the state machine. However, Wyland discloses a byte swapping unit, wherein a 32-bit input stream is demultiplexed into four 8-bit bytes, and the bytes are fed into four 2-input multiplexers, so that the bytes may be swapped in an end-to-

end manner based on a byte_endian_type control signal, whereby the output of the multiplexers are then recombined into a 32-bit stream (Wyland: Fig. 5A). Since both Baden and Wyland relate to performing byte swapping, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the multiplexer configuration of Wyland with the bridge/graphics controller of Baden in order to provide a system which is capable of operating in both an encoding/decoding mode and error correction mode while utilizing a single circuit configuration (Wyland: column 2, lines 14-17). The combined system of Baden and Wyland has all of the features of claim 12.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER FINDLEY whose telephone number is (571)270-1199. The examiner can normally be reached on Monday-Friday (8:30 AM-5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on 571-272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christopher Findley/

/Andy S. Rao/
Primary Examiner, Art Unit 2621
January 17, 2010